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(54) Subtitle signal encoding/decoding

(57) Subtitle encoding and/or decoding apparatus and corresponding method are operable to encode and/or decode multiple subtitle signals representing multiple subtitles to be superimposed on a video image. Each received subtitle signal is encoded (in the encoding apparatus only) in a coder (78) and stored in a buffer memory (82). An address list including data nodes therein is generated from the received subtitle signals wherein each data node in the address list corresponds to a respective subtitle stored in the buffer memory (82). Each data node includes data corresponding to the time and position at which a respective subtitle is to be superimposed on a video image, as well as buffer memory address information which identifies the location in the buffer memory (82) at which the respective subtitle is stored. Each data node further includes pointer data that identifies another data node that corresponds to a successively positioned subtitle in the display. Appropriate write and read address control signals are generated from the data in the address list by an address controller (84), and a subtitle signal is stored in and reproduced from the buffer memory (82) in accordance with the respective write and read address control signals. In the decoding apparatus (not shown), the read out subtitle signal is decoded before being output.

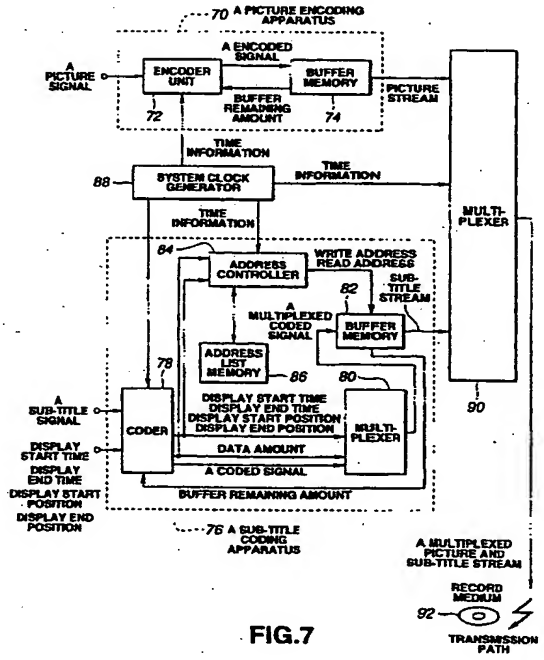

FIG.7

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signal is combined with the video signal that is output from picture decoding apparatus 44 in a combining device (not shown) such that the subtitle represented by the subtitle signal is superimposed on the video image.

Fig. 3 schematically illustrates the data stored in buffer memory 52 and the superimposition of a subtitle on a video image displayed on a monitor (i.e., a screen), wherein only one subtitle is stored in buffer memory 52 and represented by "DATA 1". When only one subtitle is superimposed on a video image, such as shown in Fig. 3, buffer memory 52 of the decoding apparatus and buffer memory 32 of the encoding apparatus each operates as a FIFO (first-in-first-out) memory.

Figs. 4 and 5 schematically illustrate when data of two subtitles are stored in buffer memory 52 and simultaneously superimposed on a video image. For example, a first subtitle, represented by "DATA 1", is displayed with the video image from a time t1 until a time t1' and is displayed at a lower portion of the image, and a second subtitle, represented by "DATA 2", is superimposed on the video image at a time t2 until a time t2' at an upper portion of the video image, such as shown in Fig. 4. Both subtitles are displayed from time t2 to time t1'. If the data "DATA 1" of the first subtitle is supplied with the video signal before the data "DATA 2" of the second subtitle is supplied, then buffer memory 52 has the data structure as shown in Fig. 5. Accordingly, when only the first subtitle is displayed (from time t1 to time t2), address controller 58 generates a read address control signal corresponding to the location in buffer memory 52 whereat DATA 1 resides. Similarly, when only the second subtitle is displayed (from time t1' to time t2'), address controller 58 generates a read address control signal corresponding to the location in buffer memory 52 whereat DATA 2 resides. However, since the second subtitle is located above the first subtitle when both subtitles are displayed (from time t2 to time t1'), it is necessary for address controller 58 to generate a read address control signal that first corresponds to the location of DATA 2 in buffer memory 52 and then to the location of DATA 1 in buffer memory 52. Thus, DATA 2 is read from buffer memory 52 before DATA 1 is read therefrom for the time period occurring between time t2 and time t1' and, thus, buffer memory 52 is not operating as a FIFO memory.

Referring next to Figs. 6A and 6B, a schematic illustration of the data structure of buffer memory 52, as well as a schematic illustration of the times and positions at which four different subtitles are displayed. A first subtitle "DATA 1" is stored in buffer memory 52 and displayed at an upper portion of the video image, a second subtitle "DATA 2" is stored after DATA 1 in buffer memory 52 and is displayed at a middle portion of the video image at a time when the first subtitle is still being displayed. Upon termination of the display of the first subtitle, subtitle data DATA 1 corresponding thereto is erased from buffer memory 52, and a third subtitle DATA 3 is stored after DATA 2 in buffer memory 52 and displayed above the second subtitle in the video image. At this time, DATA 3 is read from buffer memory 52 before DATA 2 is read therefrom. A fourth subtitle DATA 4 subsequently is stored after DATA 3 in buffer memory 52 and DATA 3 is read from memory, then DATA 2 is read from memory, and then DATA 4 is read from memory for each frame until the termination of the display of the third subtitle DATA 3, at which time the third subtitle DATA 3 is erased from buffer memory 52, as shown. The display of the second subtitle DATA 2 then is terminated and DATA 2 is erased from buffer memory 52 and, subsequently, the display of the fourth subtitle DATA 4 is terminated and DATA 4 is erased from buffer memory 52. As can be appreciated from the foregoing description, buffer memory 52 cannot be controlled to operate as a FIFO type memory. Further, subtitle data are not consecutively stored in buffer memory 52 at each instance in time as shown in Fig. 6B. Still further, due to the complex control of buffer memory 52 and since subtitle data are not consecutively stored therein, the control of buffer memory 32 of the coding apparatus shown in Fig. 1 does not coincide with the control of buffer memory 52 of the decoding apparatus shown in Fig. 2. Thus, overflow and/or underflow of data stored in buffer memories 32 and 52 is possible, which results in the inherent limiting of the number of subtitles that can be displayed on a video image and the arrangement thereof.

In accordance with one embodiment of the present invention, apparatus and method are provided for receiving a subtitle signal which represents a subtitle to be superimposed on a video image, encoding the subtitle signal, generating an address list from the display time and display position data which are included in the subtitle signal and which represent a time and position at which the subtitle is to be superimposed on the video image, generating a write address signal, generating a read address signal in accordance with the generated address list, storing the coded subtitle signal in a memory in accordance with the write address signal, reading the stored coded subtitle signal from the memory in accordance with the read address signal, and supplying as an output signal the coded subtitle signal read from the memory.

As one aspect of the present invention, a data node is added to the address list each time a new subtitle (i.e., subtitle signal) is received, wherein the added data node includes data that corresponds to the display time and position data included in the newly received subtitle signal and also includes memory location data which represents a location in the memory at which the newly received subtitle signal is stored.

As a feature of this aspect, each data node in the address list further includes respective pointer data that identifies another data node in the address list that corresponds to a subtitle that is to be superimposed positionally after the subtitle that corresponds to the respective data node.

Read address signals may be generated that cor-

data amount signal and the time and position data to address controller 84 which generates an address list therefrom (to be discussed) and stores the address list in address list memory 86. Address controller 84 further generates write and read address control signals from the address list stored in memory 86 (also to be discussed) and supplies the write and read address control signals to buffer memory 82. Buffer memory 82 stores the multiplexed coded signal supplied thereto at a memory address therein as indicated in the write address control signal and reads data from an address as indicated in the read address control signal and supplies the read out data as a subtitle stream to multiplexer 90. Buffer memory 82 further supplies a control signal representing the amount of unused memory in the buffer to encoder 78 which, in response thereto, codes the subtitle signal in a manner well known in the art to prevent overflow or underflow of data in buffer memory 82.

System clock generator 88 supplies time information (i.e., a system clock signal) to encoder unit 72, coder 78, address control 84 and multiplexer 90 and these devices are controlled to operate in a synchronous manner. Multiplexer 90 multiplexes the picture stream signal supplied from picture encoding apparatus 70 and a subtitle stream supplied from subtitle coding apparatus 76, and supplies the multiplexed signal for transmission thereof over a transmission path or, alternatively, to a recording device (not shown) which records the multiplexed signal on a record medium 92.

Fig. 8 is a block diagram of a decoding apparatus which is comprised of a picture decoding apparatus 96 and a subtitle decoding apparatus 102 in accordance with the present invention. Picture decoding apparatus 96 is comprised of a buffer memory 98 and a decoder unit 100, and operates in a manner similar to that of picture decoding apparatus 44 shown in Fig. 2 and, thus, further description thereof is omitted herein except where necessary for an understanding of the present invention.

Subtitle decoding apparatus 102, in accordance with the present invention, is comprised of a buffer memory 104, a demultiplexer 106, a decoder 108, an address controller 110 and an address list memory 112. The coded multiplexed picture and subtitle signal is received over a transmission path, or alternatively, is reproduced from record medium 92 in a reproducing device (not shown), and the coded multiplexed signal is supplied to a demultiplexer 94 which demultiplexes the signal into its coded picture and coded subtitle components. The coded picture signal is supplied as a picture stream to picture decoding apparatus 96 which temporarily stores the picture stream in buffer memory 98 and decodes in decoder unit 100 the coded signal in a manner well known in the art. The decoded picture signal is supplied as an output signal at a time as controlled by a time information signal supplied from a system clock generator 114.

Demultiplexer 94 supplies the coded subtitle signal to buffer memory 104 in subtitle decoding apparatus 102 which stores the supplied signal at a memory address therein as indicated in a write address control signal supplied from address controller 110. Buffer memory 104 reads the stored subtitled data from a memory address as indicated in a read address control signal supplied from address controller 110 and supplies the read out signal to demultiplexer 106 which demultiplexes the subtitle data into its respective coded subtitle signal, data amount signal, and time and position signal components. The coded subtitle signal, data amount signal and time and position signals are supplied to decoder 108 which decodes the respectively supplied signals in a manner well known in the art and which supplies a decoded subtitle signal representing a subtitle to be superimposed on a video image at an appropriate time as indicated by the time and position data supplied thereto.

Address controller 110 generates from the supplied time and position data an address list (to be discussed) and supplies the generated address list to address list memory 112 which stores the address list therein. Address controller 110 further generates the write and read address control signals from the address list stored in memory 112 as well as from the time information supplied from system clock generator 114, and supplies the generated write and read address control signals to buffer memory 104.

The generation of an address list by both address controller 84 of the subtitle coding apparatus and address controller 110 of the subtitle decoding apparatus will now be discussed with reference to Figs. 9, 10 and 11A - 11C. However, for purposes of the present discussion, since the operation of address controllers 84 and 110 are substantially similar, the discussion herein will be directed to the operation of address controller 110, but it is understood that the functions and operations of address controller 110 also are applicable to address controller 84.

When two subtitles are supplied with the video picture, a first subtitle, represented by "DATA 1", is stored in buffer memory 104 at a first memory address therein, as shown in the left hand portion of Fig. 9. Address controller 110 generates appropriate write address control signals so that buffer memory 104 successively stores the subtitle data of the first subtitle (DATA 1) at a top memory address (or first memory address) of buffer memory 104. Upon receipt of the first subtitle data (and storage thereof in buffer memory 104), address controller 110 generates a first data "node" which contains various data including the first and last addresses (start address and end address) of buffer memory 104 at which the first subtitle DATA 1 is stored, the display start and end times at which the first subtitle is to be superimposed on the video image, and the display start and end positions at which the first subtitle is to be superimposed on the video image. The first node is illustrated in Fig. 10 as the "node of DATA 1". The DATA 1 node (as well as all other nodes, as will be seen) further includes

buffer memory 104, decoded and superimposed on the video image. In addition, at display end time t1', the first subtitle is erased from buffer memory 104 (to be discussed) and the first node corresponding to the first subtitle is erased from the address list, and the pointers of each of the remaining nodes in the address list are reestablished, such as shown in Fig. 11C. Only the second subtitle now is stored in buffer memory 104, and, therefore, the initial pointer points to the second node and the pointer of the second node points to the end pointer.

The operation of the subtitle decoding apparatus of the present invention when four subtitles are supplied with the video signal will now be discussed with reference to Figs. 12A and 12B. As shown in Fig. 12A, the first subtitle DATA 1 is supplied to and stored in buffer memory 104. Fig. 12B illustrates the data structure of buffer memory 104, wherein the first subtitle DATA 1 is stored at a beginning memory location therein. At this time, an address list is generated in address controller 110 which includes a first node corresponding to the first subtitle DATA 1, and at the display start time of the first subtitle, the first subtitle is superimposed on the video image. The second subtitle DATA 2 subsequently is supplied to and stored in buffer memory 104, and a second node corresponding to the second subtitle is added to the address list, wherein the pointer of the first node points to the second node since the second subtitle positionally occurs after the first subtitle in the video image. Then, both the first and second subtitles are superimposed on the video image at the display start time of the second subtitle. When the display end time t1' of the first subtitle is reached (not shown in Fig. 12B), the first subtitle DATA 1 is erased from buffer memory 104 and the first node is removed from the address list, and the initial pointer is set to point to the second node of the address list.

When a third subtitle DATA 3 is supplied to buffer memory 104, it is stored immediately after the second subtitle therein, and a third node corresponding to the third subtitle is added to the address list. Also, and as previously discussed, the pointers of each of the nodes (i.e., nodes 2 and 3) are established such that the initial pointer points to the third node and the pointer of the third node points to the second node. When the display start time t3 of the third subtitle is reached, both the third and second subtitles are superimposed on the video image.

When a fourth subtitle DATA 4 is supplied to buffer memory 104, it is stored after the third subtitle therein and a fourth node is added to the address list. Further, since the fourth subtitle positionally occurs after the second subtitle in the video image, the pointer of the second node is established to point to the fourth node, and the pointer of the fourth node is established to point to the end pointer. When the display start time t4 of the fourth subtitle is reached, the third, second and fourth subtitles each are read from buffer memory 104 (in this order), decoded and superimposed on the video image.

As shown in Figs. 12A and 12B, at the display end time t3' of the third subtitle, the superimposition of the third subtitle on the display is terminated, but the third subtitle is not erased from buffer memory 104 and the third node is not removed from the address list for reasons to be discussed. When the display end time t2' of the second subtitle is reached, both the second and third subtitles are erased from buffer memory 104 and the second and third nodes are removed from the address list, as shown in Fig. 12B. Then, since only the fourth subtitle is stored in buffer memory 104, the initial pointer is established to point to the fourth node. Finally, when the display end time t4' of the fourth subtitle is reached, the fourth subtitle is removed from buffer memory 104 and the fourth node is removed from the address list (not shown in Fig. 12B).

As mentioned above, when the display end time t3' of the third subtitle is reached, the third subtitle is not erased from buffer memory 104 and the third node is not removed from the address list. In accordance with the present invention, when subtitle data exists in buffer memory 104 which precedes a "current" subtitle which superimposition thereof on a video image has just been terminated, the "current" subtitle is not removed from memory and the node corresponding to the "current" subtitle is not removed from the address list. The present invention seeks to operate buffer memory 104 as a FIFO type memory device which provides several advantageous features to the present invention. For example, overflow or underflow of data in the buffer is prevented by the aforementioned operation since a signal representing the amount of unused memory in the buffer memory (produced thereby) represents a true value of useable space that is available for other subtitle data. As another example, leaving the above-discussed subtitle data in buffer memory 104 even after the termination of the display of the subtitle simplifies the control of the buffer memory.

Thus, and in accordance with the present invention, a subtitle is erased from buffer memory 104 upon termination of the display thereof if no data precedes that subtitle in memory. In addition, if data (i.e., subtitle data) exists that precedes the subtitle (which display thereof is terminated) represents a subtitle (or subtitles) which display thereof already is terminated, then both of these subtitles are erased from buffer memory 104 and the nodes corresponding thereto are removed from the address list. The cases in which subtitle data is erased or is not erased from buffer memory 104 is further described below with reference to Figs. 14-17.

Fig. 13 is a flow chart of the operation of both address controller 84 of subtitle coding apparatus 76 (Fig. 7) and address controller 110 of subtitle decoding apparatus 102 (Fig. 8) when one or more subtitles are supplied thereto. The operation begins at instruction S1 and, at inquiry S2, it is determined whether a new subtitle is received. In the subtitle coding apparatus 76, a new subtitle is received when it is provided to coder 78,

node corresponding to that subtitle is removed from the address list at instruction S44. Then, or if the display of the successive subtitle is not terminated, the process proceeds back to inquiry S32.

Fig. 16 is a flow chart of the operation of address controller 84 of subtitle coding apparatus 76 when two subtitles are supplied thereto. The flow chart of Fig. 16 is substantially similar to the flow chart of Fig. 14, which represents the operation of address controller 110 of subtitle decoding apparatus 102 when two subtitles are supplied, in that inquiry S52, instructions S53-S54, inquiry S55 and instruction 58 are the same as inquiry S22, instructions S23-S24, inquiry S25 and instruction S27, respectively. Therefore, a description thereof is omitted herein. However, when address controller 84, at inquiry S55, determines that a currently processed subtitle (i.e., node) is to currently displayed, then it is determined at inquiry S56, if the current time, as indicated by the system clock signal, represents the display start time of the current subtitle. If so, the subtitle is read from buffer memory 82 and subsequently multiplexed with the video image for recording or transmission thereof. If not, the process proceeds back to inquiry S52. Thus, address controller 84 operates to control buffer memory 82 in subtitle coding apparatus 76 to supply a subtitle for multiplexing with the video signal at the time when that subtitle is to be superimposed on the video image.

Referring next to Figs. 17A and 17B, a flow chart of the operation of address controller 84 when three or more subtitles are provided is shown. The flow chart of Figs. 17A - 17B is substantially the same as the flow chart of Figs. 15A - 15B and, thus, a description of those instructions and inquiries that are the same therein are omitted herein. However, in the flow chart of Figs. 17A - 17B, when it is determined at inquiry S65 that a current subtitle is to be displayed, the process proceeds to inquiry S66 at which time it is determined whether the current time, as indicated by the system clock signal, is equal to the display start time of the subtitle. If so, the current subtitle is read from buffer memory 82 in a manner similar to that discussed above with reference to the flow chart of Fig. 16. If not, the process proceeds to inquiry S62. In addition, it is determined, at inquiry S70, if the preceeding subtitle in buffer memory 82 is being displayed, and if so, the current subtitle is not displayed (and not erase from memory), at instruction S71.

From the above discussion, it is seen that both buffer memories 82 and 104 are controlled to operate as first-in-first-out memory devices so that the control thereof may be simplified and, further, so as to prevent the underflow/overflow of data therein. By using an address list which includes nodes which each corresponds to a respective subtitle stored in the buffer memories, and by providing in each node various subtitle data including the display start and end time data, the display start and end position data, and the start and end addresses at which the subtitle data is stored, as well as a pointer which points to a successive subtitle that is to be displayed positionally on the video image, allows for the simplified processing and control of a multiple number of subtitles.

While the present invention has been particularly shown and described in conjunction with preferred embodiments thereof, it will be readily appreciated by those of ordinary skill in the art that various changes may be made without departing from the spirit and the scope of the invention. For example, although the specific block structure of the subtitle coding and decoding apparatus has been shown and described, the present invention is not limited to this specific block structure and may be applied to other types of block structures and circuits which involve the superimposition or display of subtitles or other video data.

Therefore, it is intended that the appended claims be interpreted as including the embodiments described herein, the alternatives mentioned above, and all equivalents thereto.

Claims

1. Apparatus for coding a subtitle signal, comprising:

   means for receiving a subtitle signal representing a subtitle to be superimposed on a video image, said subtitle signal including display time data representing a time at which said subtitle is to be superimposed and display position data representing a location in said video image at which said subtitle is to be superimposed;
   encoding means for encoding the received subtitle signal to produce a coded subtitle signal;
   storage means for temporarily storing the coded subtitle signal in accordance with a write address signal and for reading out the stored coded subtitle signal in accordance with a read address signal;
   storage control means for generating an address list from said display time data and said display position data and for generating said read address signal and said write address signal in accordance with the generated address list; and
   means for supplying as an output signal the coded subtitle signal read from said storage means.

2. The apparatus of claim 1, wherein said storage control means is operable to add a data node to said address list each time a subtitle signal representing a respective subtitle is received, said data node including data corresponding to said display time data and said display position data included in said subtitle signal, said data node further including memory location data representing a location in said storage

trol means is operable to generate appropriate write address signals such that successively received coded subtitle signals representing respective subtitles are stored in successive locations in said storage means, said storage control means being further operable to generate appropriate read address signals such that selected coded subtitle signals in accordance with their respective display time data are read from said storage means; and said storage control means being further operable to remove from said storage means a coded subtitle signal having respective display time data representing an end time that is earlier than a current time only if there is no coded subtitle signals preceding said respective coded subtitle signal in said storage means.

14. The apparatus of claim 8, wherein the storage control means generates said read address signal and said write address signal such that said storage means operates as a first-in-first-out memory.

15. Method of coding a subtitle signal, comprising the steps of:

receiving a subtitle signal representing a subtitle to be superimposed on a video image, the subtitle signal including display time data representing a time at which the subtitle is to be superimposed and display position data representing a location in the video image at which the subtitle is to be superimposed;
encoding the received subtitle signal to produce a coded subtitle signal;
generating an address list from the display time data and the display position data;
generating a write address signal;
generating a read address signal in accordance with the generated address list;
storing the coded subtitle signal in a memory in accordance with the write address signal;
reading the stored coded subtitle signal from the memory in accordance with the read address signal; and
supplying as an output signal the coded subtitle signal read from the memory.

16. The method of claim 15, further comprising the step of adding a data node to the address list each time a subtitle signal representing a respective subtitle is received, each said data node including data corresponding to the display time data and the display position data included in the respective subtitle signal, each said data node further including memory location data representing a location in the memory at which the respective coded subtitle signal is stored.

17. The method of claim 16, wherein each said data node in the address list further includes respective pointer data identifying another one of said data nodes in the address list corresponding to a subtitle to be superimposed positionally after the subtitle corresponding to the respective data node.

18. The method of claim 17, wherein said step of generating a read address signal is carried out by generating a read address signal corresponding each coded subtitle that is to be read from the memory in an order as indicated by the respective pointer data of each said data node in the address list.

19. The method of claim 17, wherein said step of generating a read address signal is carried out by determining, for each data node stored in the address list in an order as indicated by the respective pointer data of each said data node, whether a respective coded subtitle signal stored in the memory is to be output as a function of a system clock time and the respective display time data included in the respective data node and generating a read address signal corresponding only to each respective coded subtitle signal that has been determined to be output.

20. The method of claim 15, wherein said step of generating a write address signal is carried out by generating appropriate write address signals such that successively received and coded subtitle signals representing respective subtitles are stored in successive locations in the memory; and said step of generating a read address signal is carried out by generating appropriate read address signals such that selected coded subtitle signals in accordance with their respective display time data are read from the memory; said method further comprising the step of removing from the memory a stored coded subtitle signal having respective display time data representing an end time that is earlier than a current time only if there is no coded subtitle signals preceding the respective coded subtitle signal in the memory.

21. Method of decoding a coded subtitle signal, comprising the steps of:

receiving a coded subtitle signal representing a subtitle to be superimposed on a video image, the coded subtitle signal including display time data representing a time at which the subtitle is to be superimposed and display position data representing a location in the video image at which the subtitle is to be superimposed;
generating an address list from the display time data and the display position data;
generating a write address signal;
generating a read address signal in accordance

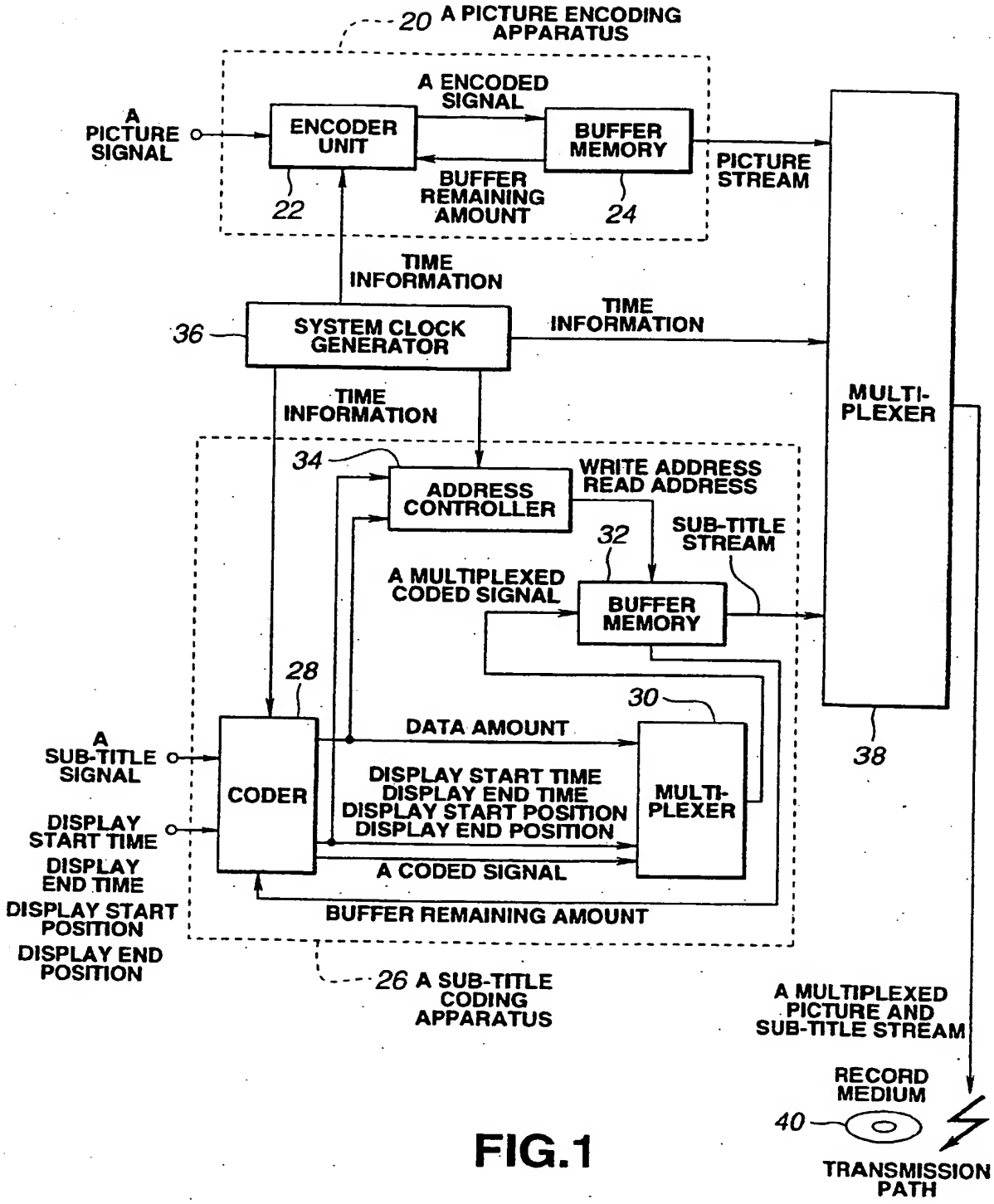

FIG.1

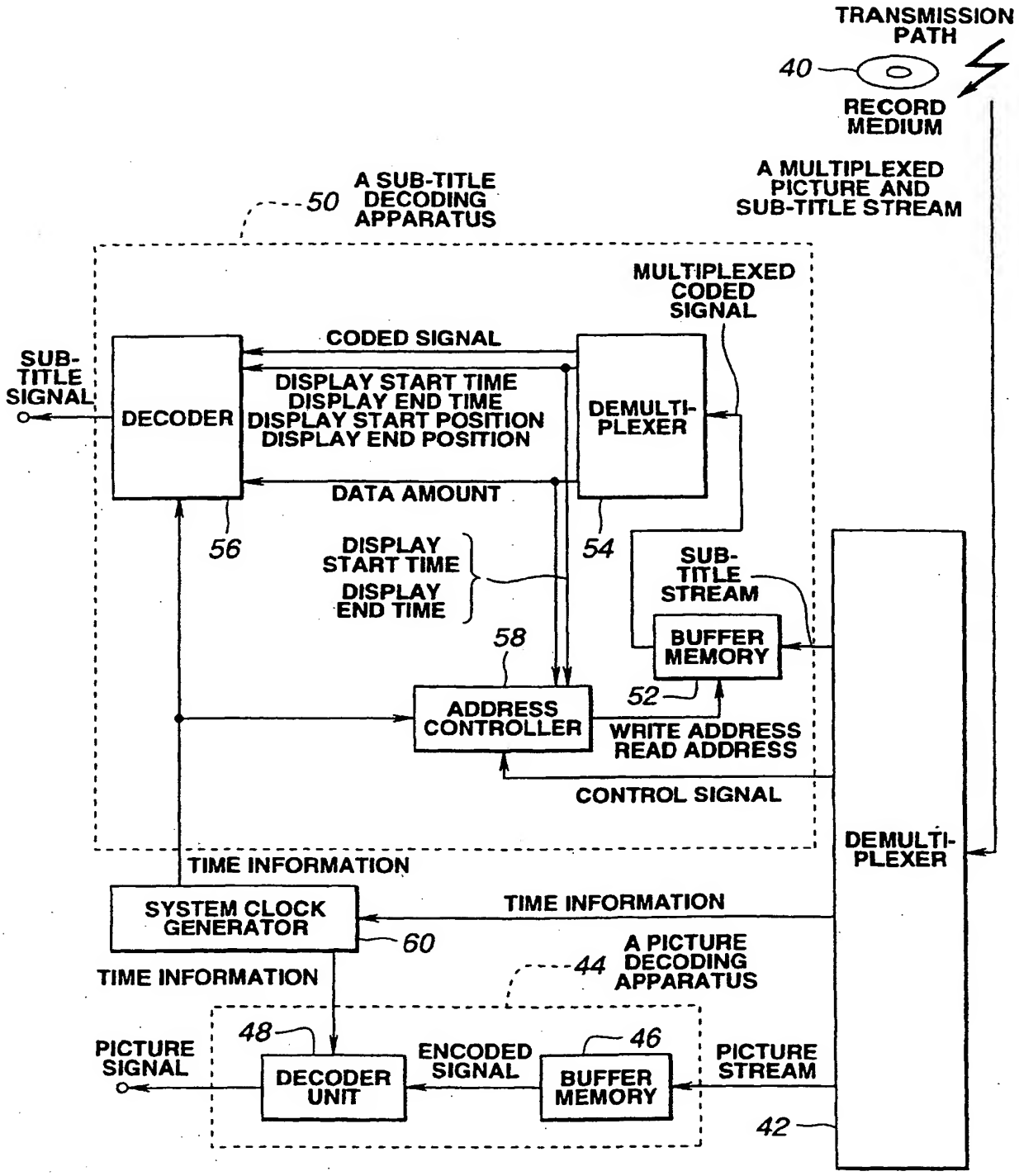

FIG.2

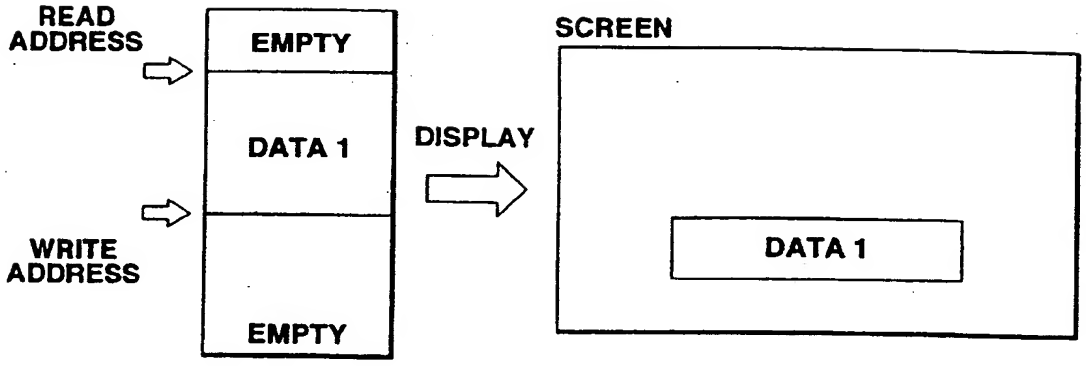

FIG.3

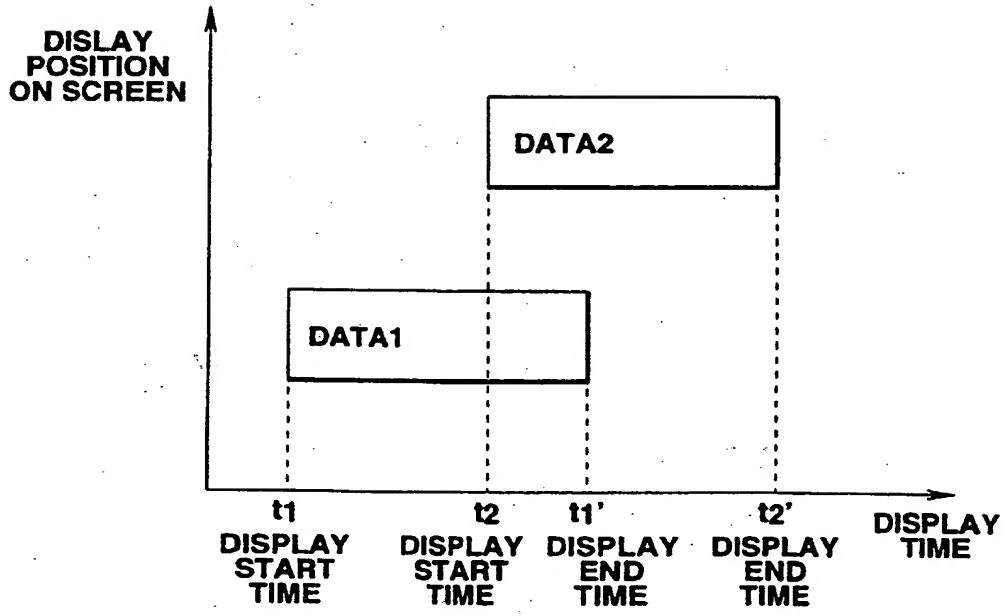

FIG.4

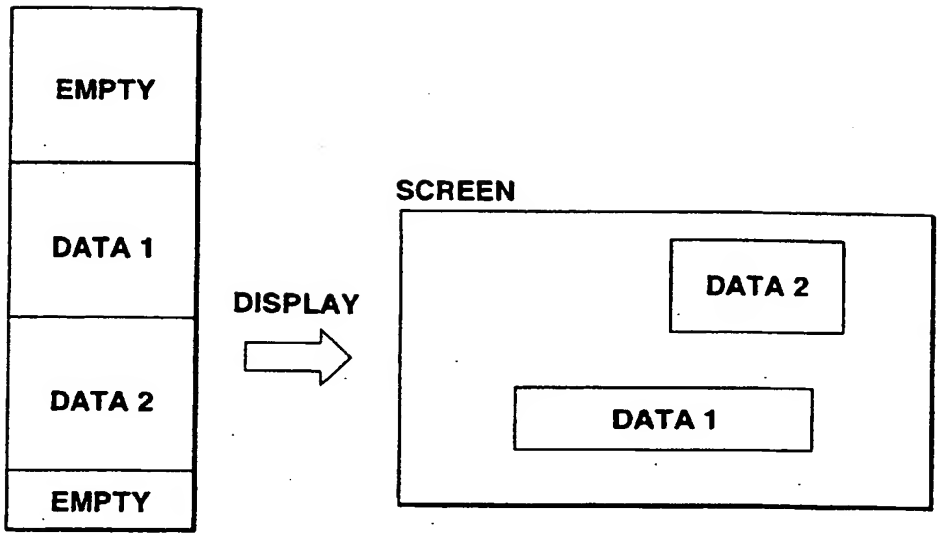

FIG.5

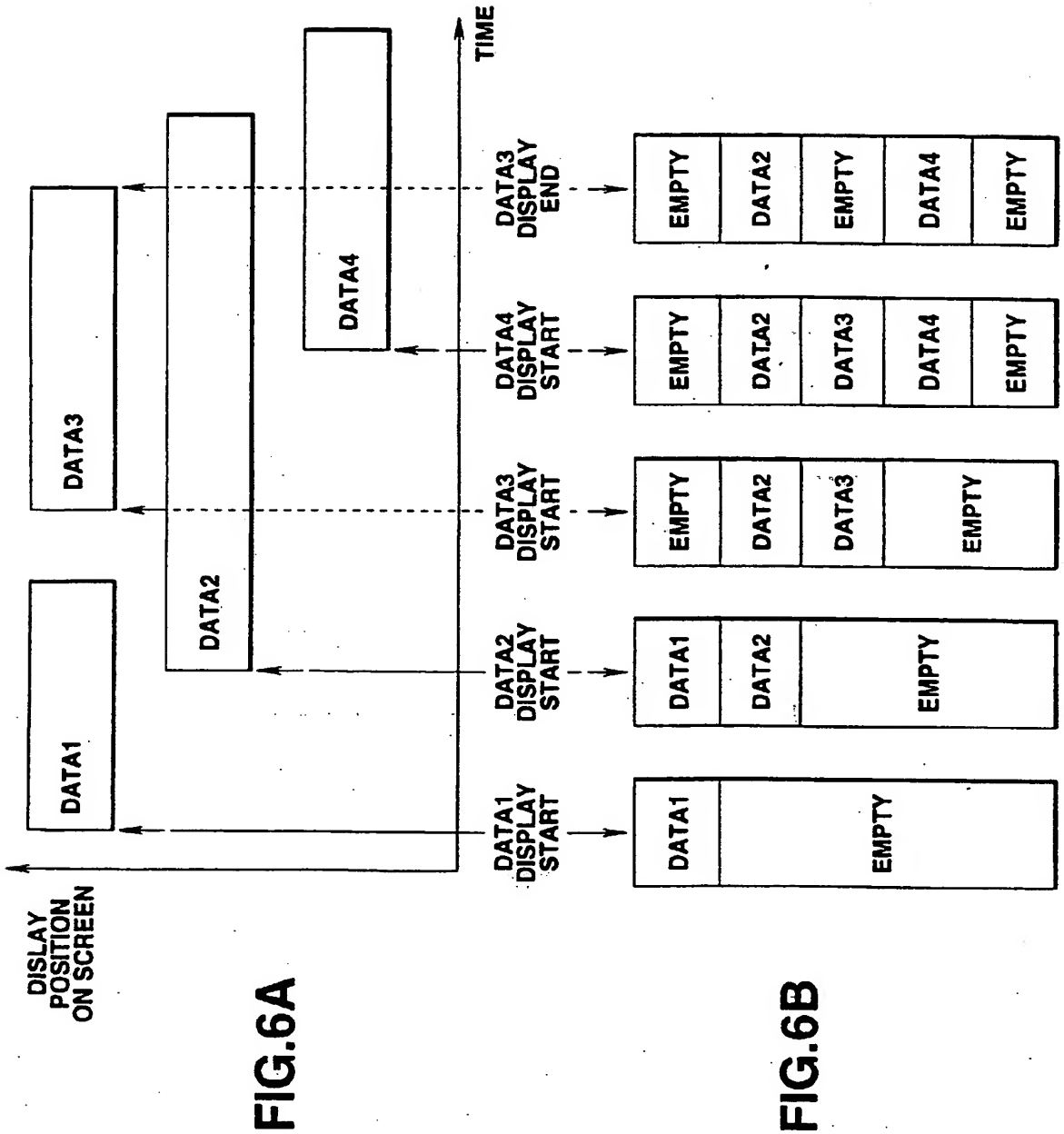

FIG.6A

FIG.6B

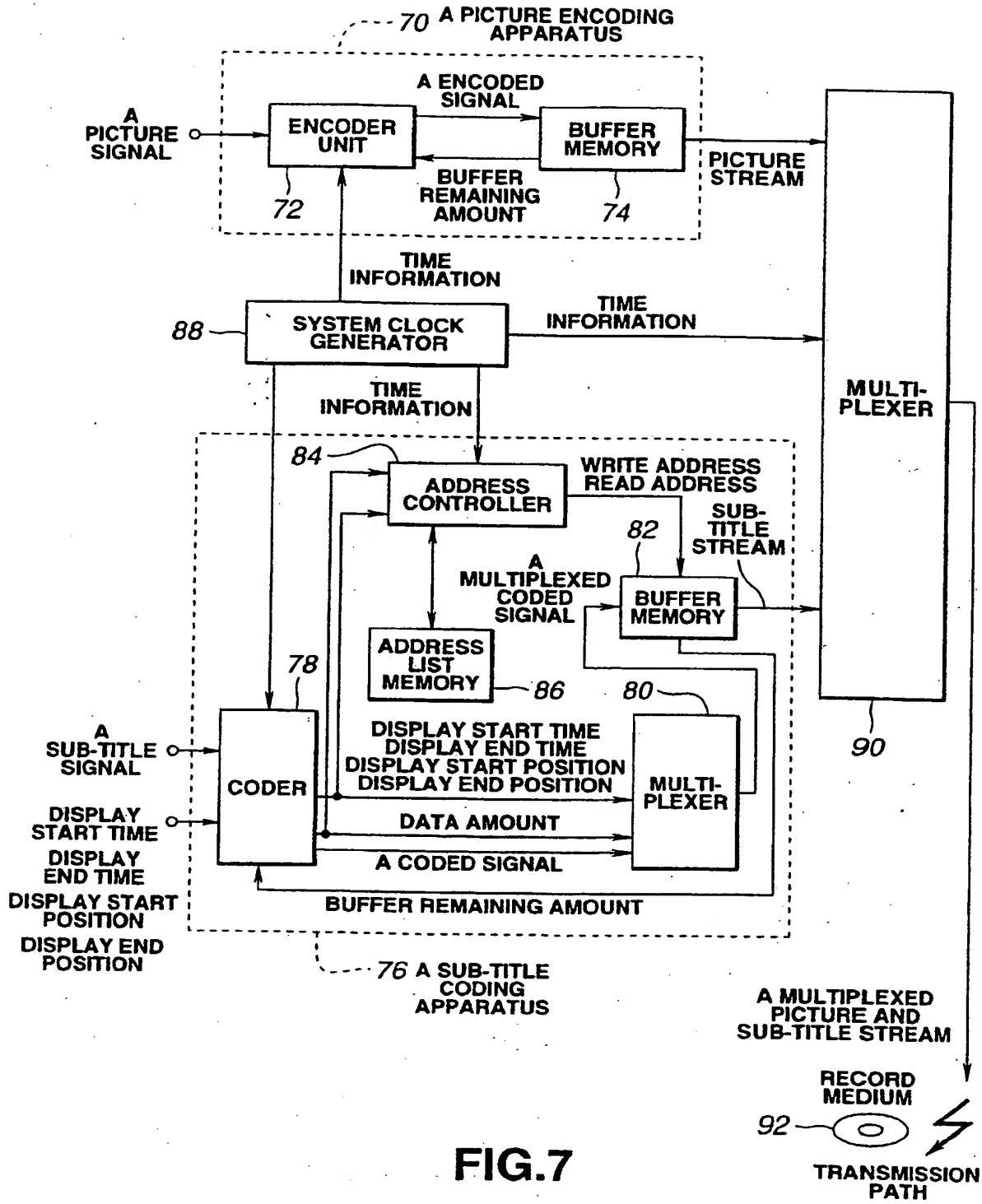

FIG.7

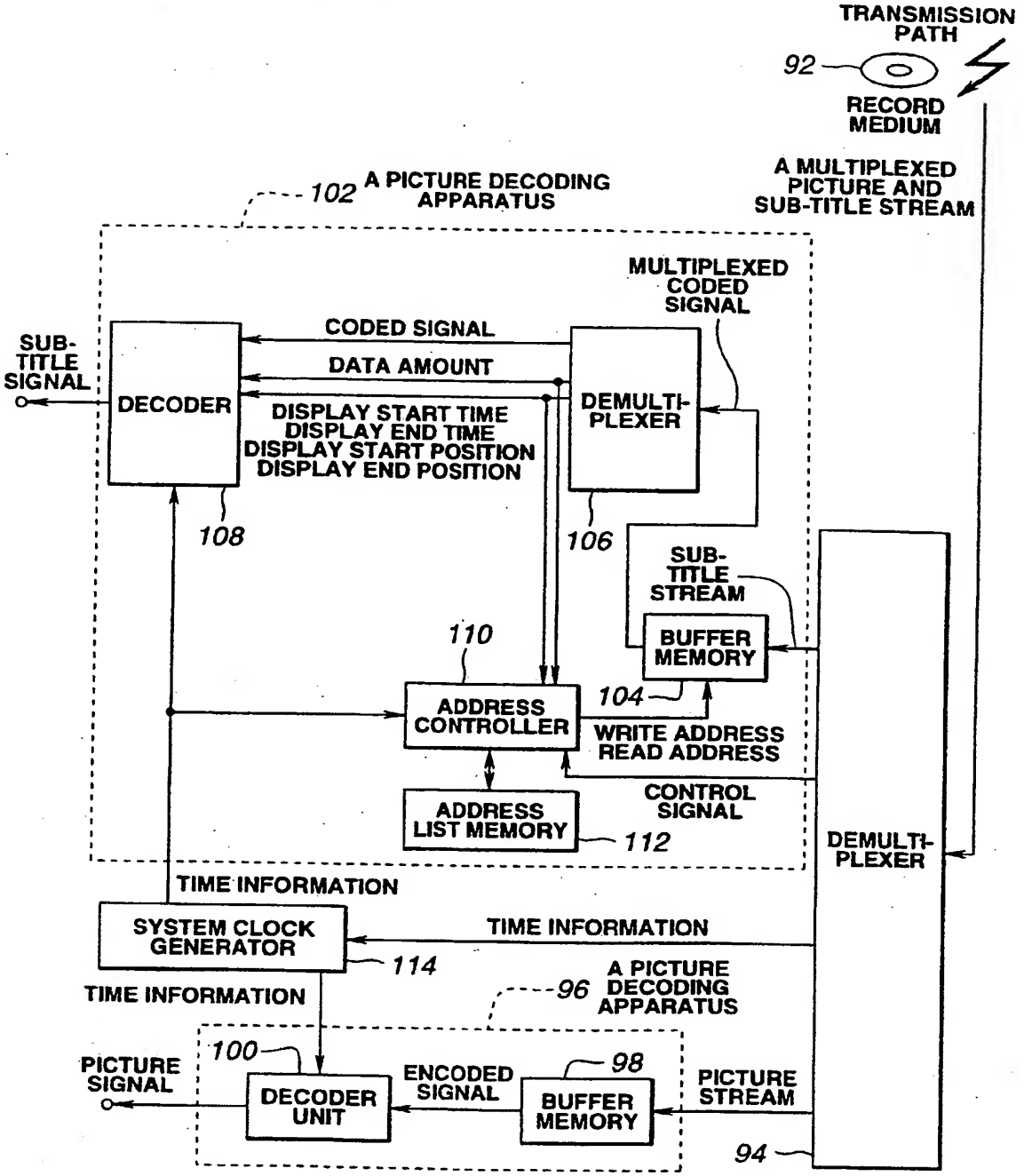

FIG.8

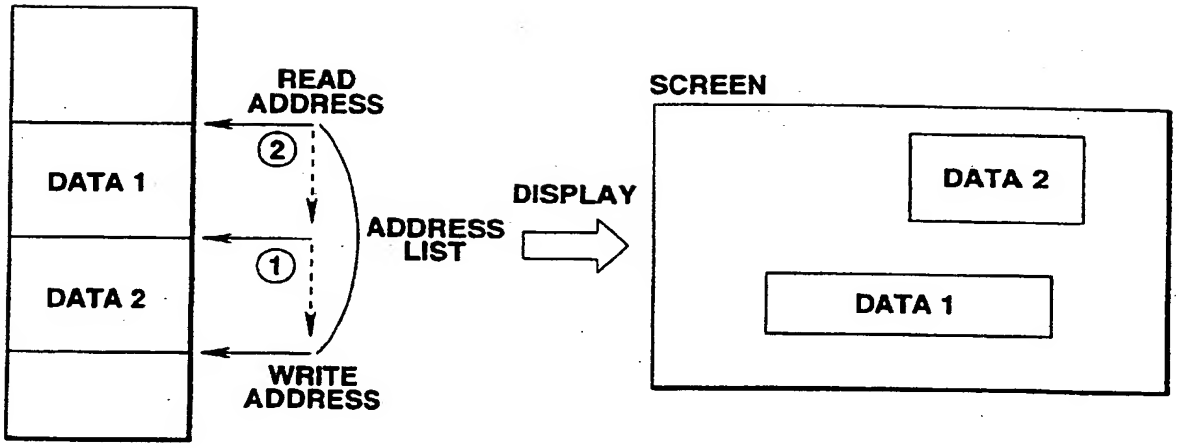

FIG.9

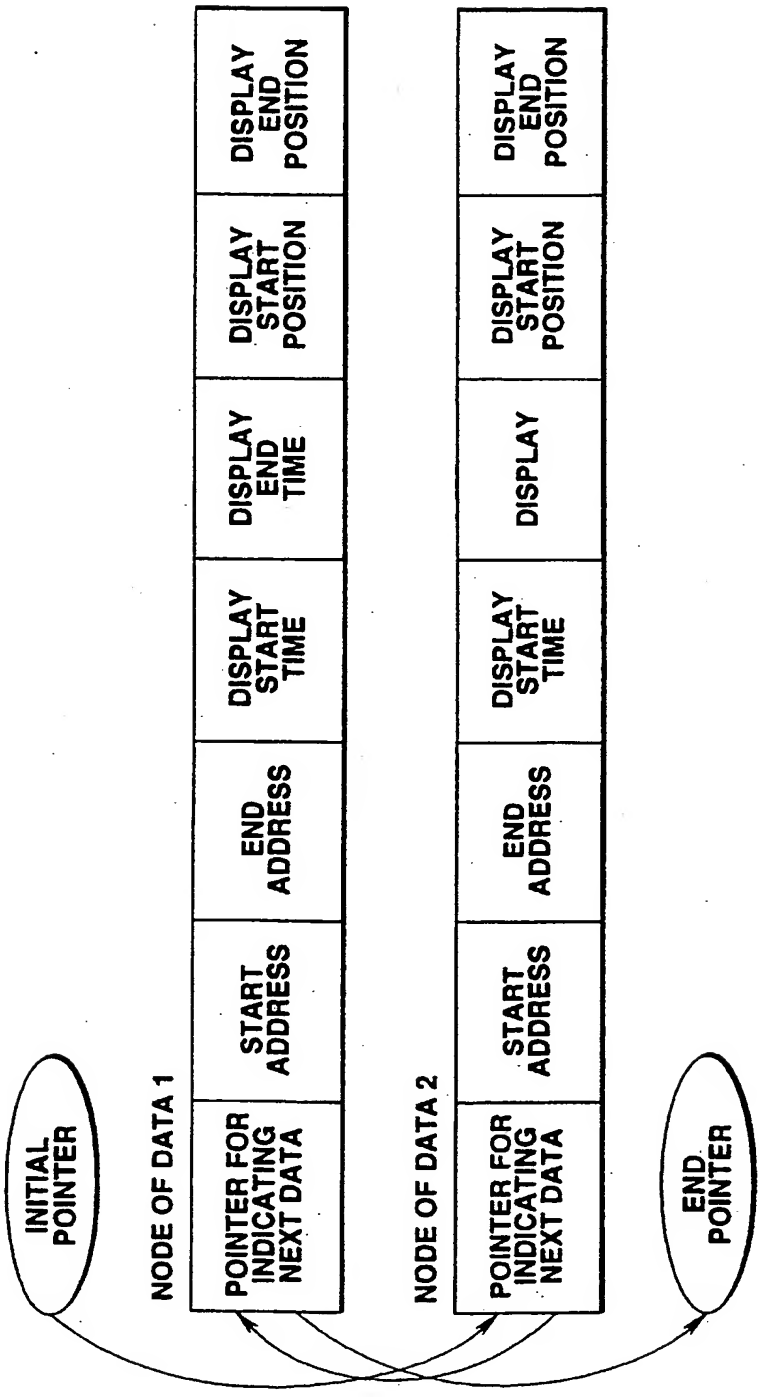

FIG.10

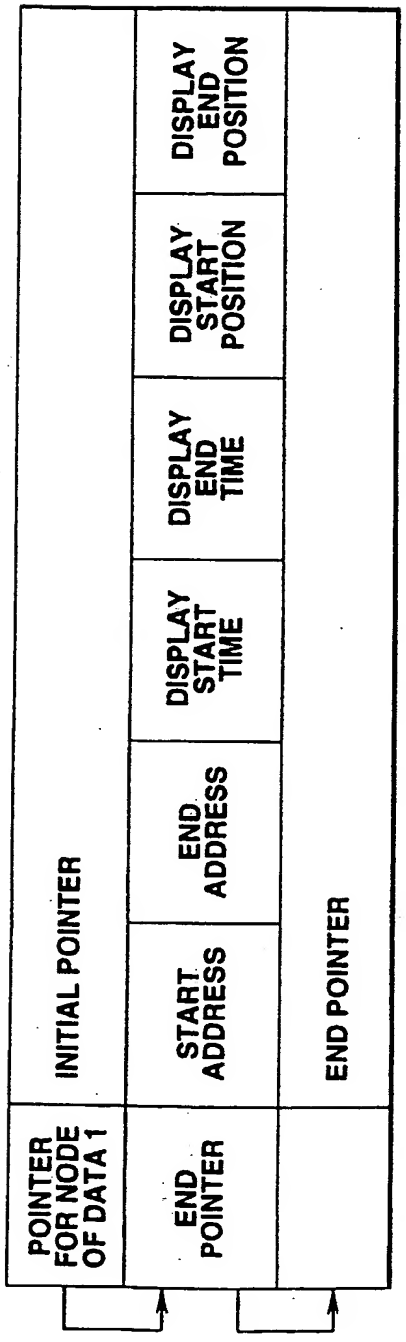

FIG.11A

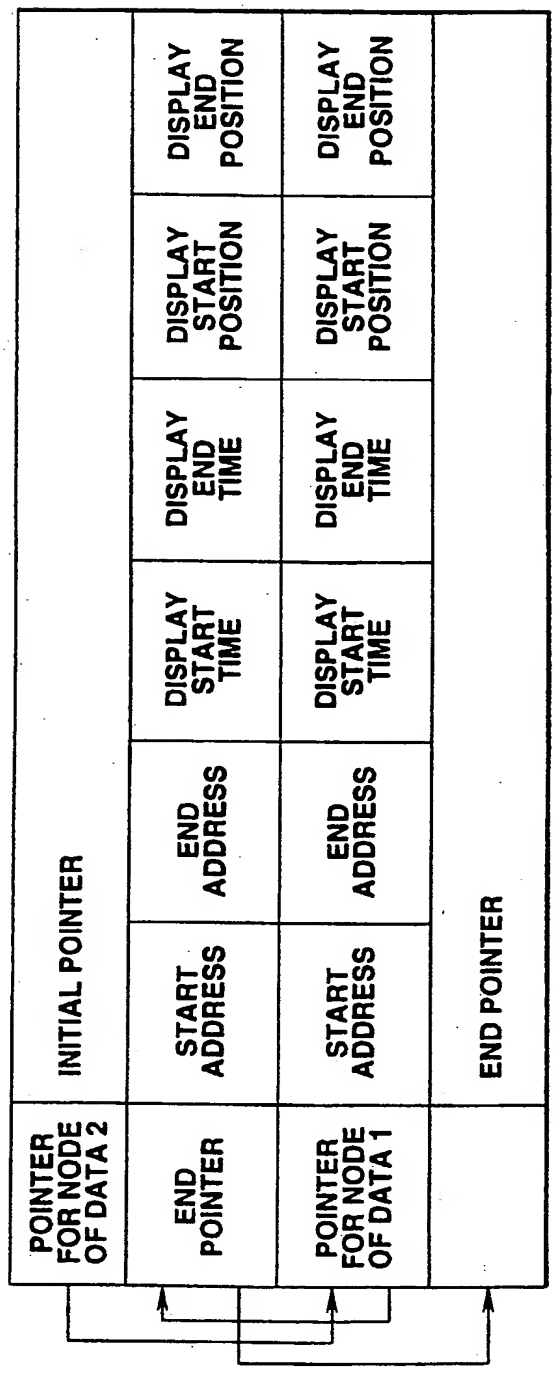

FIG.11B

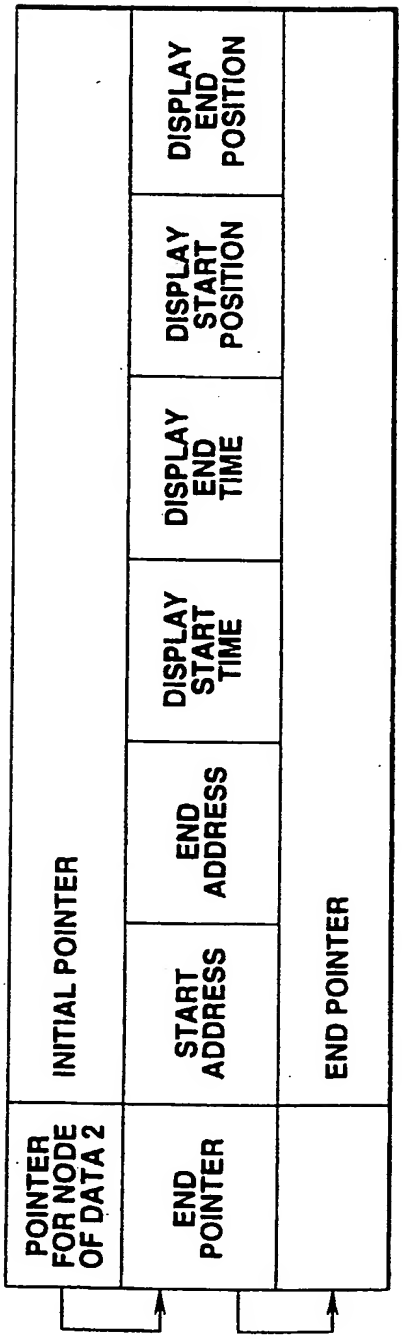

FIG.11C

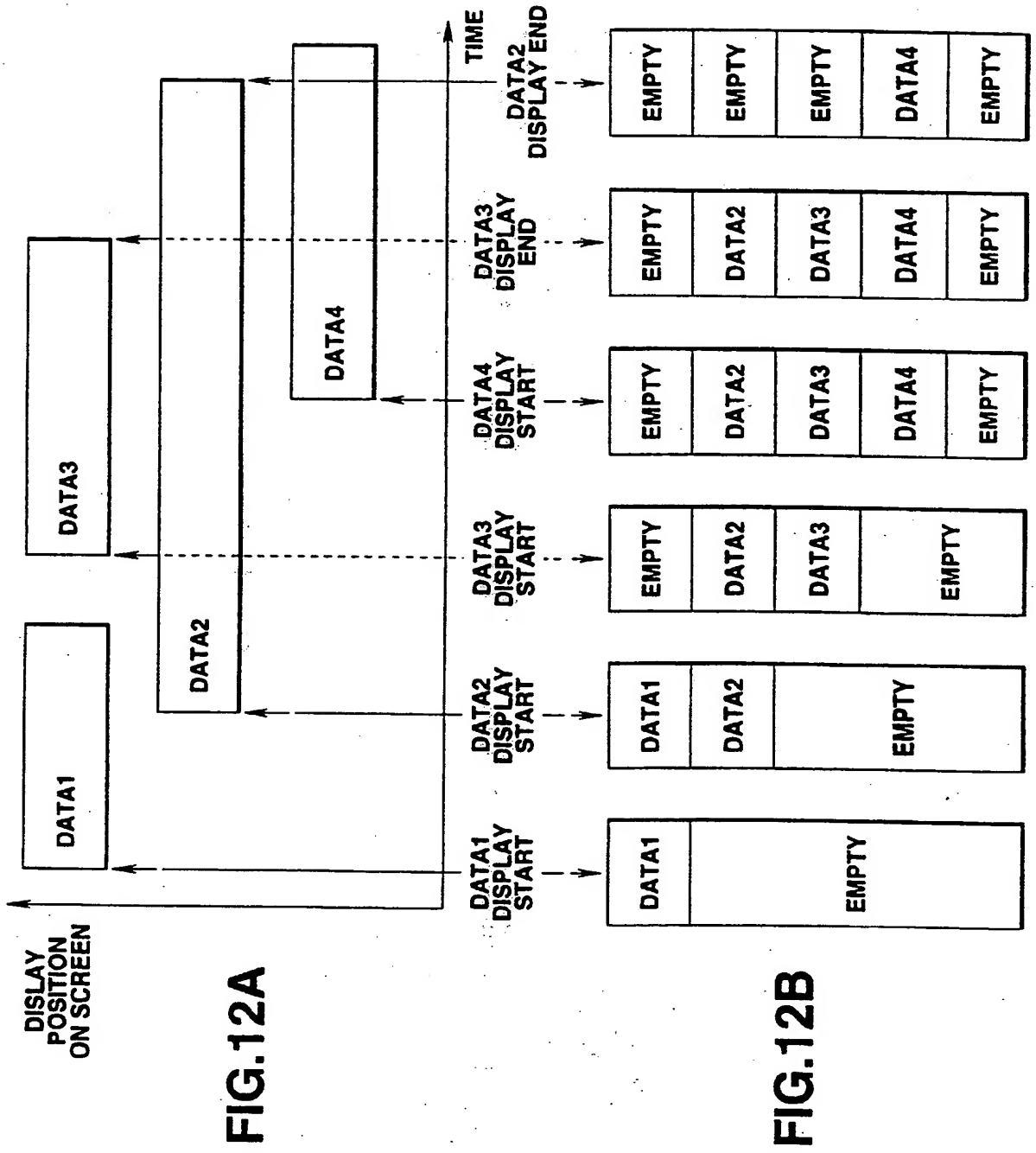

FIG.12A

FIG.12B

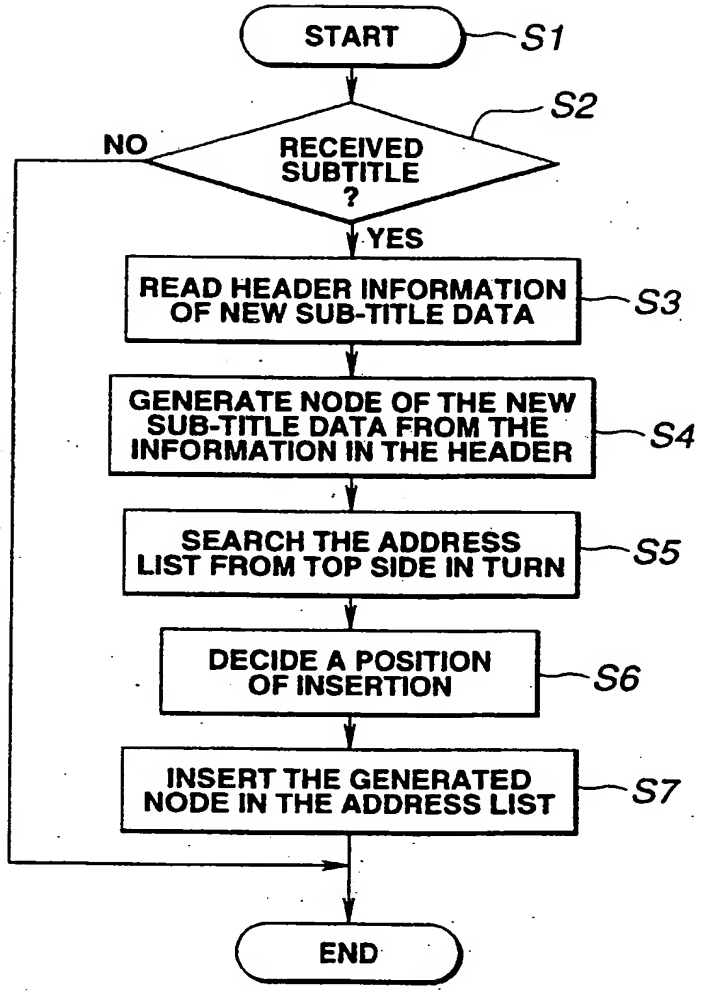

FIG.13

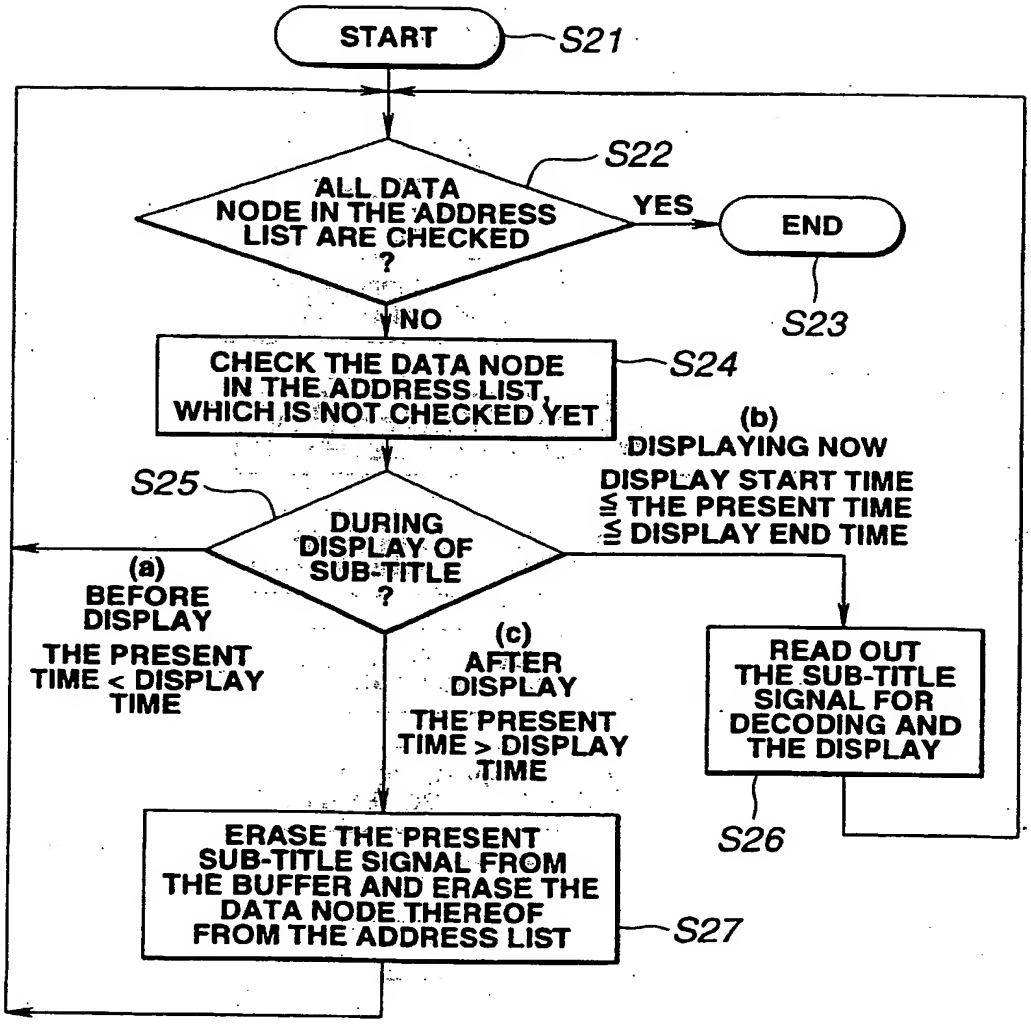

FIG.14

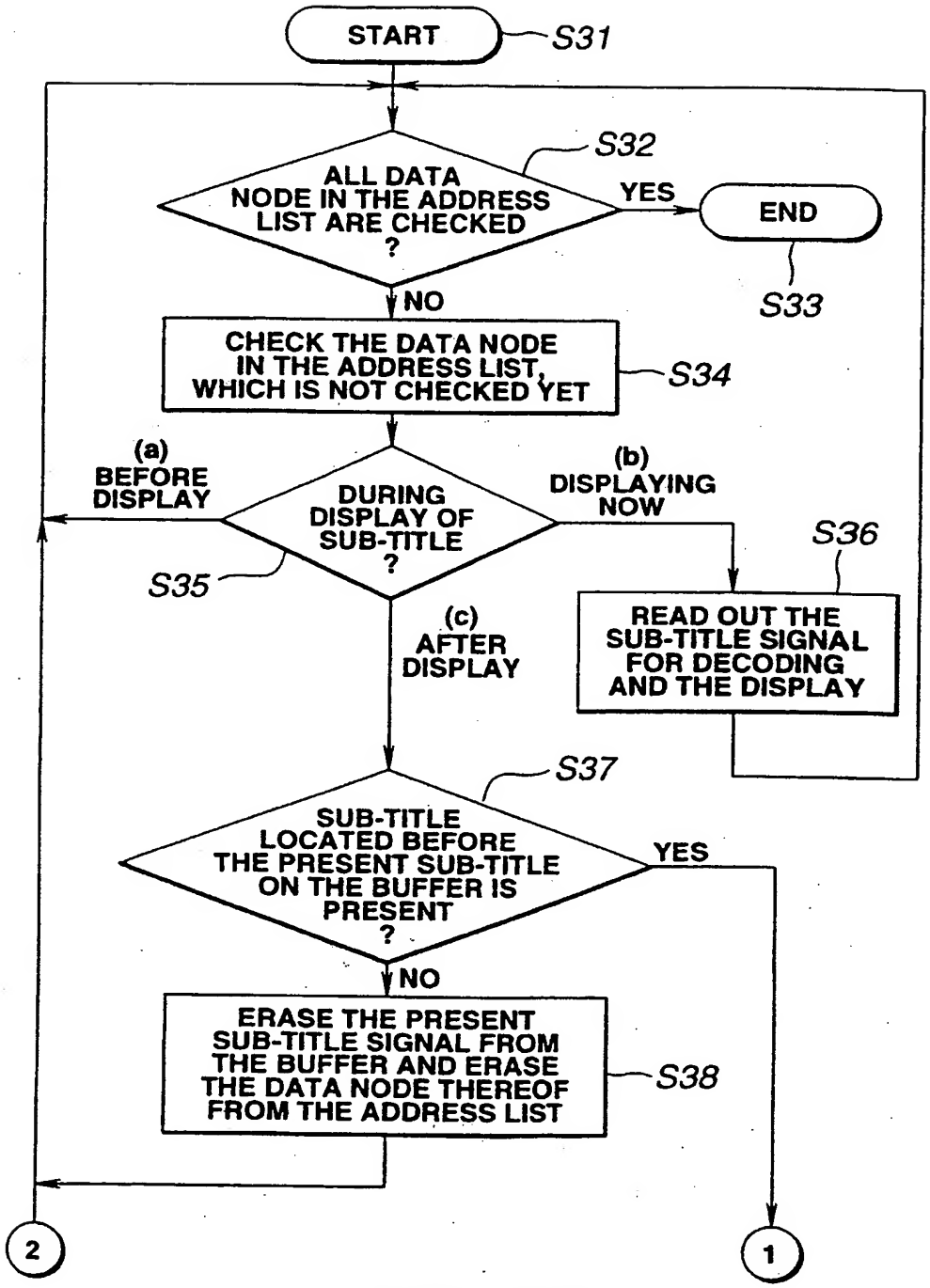

FIG.15A

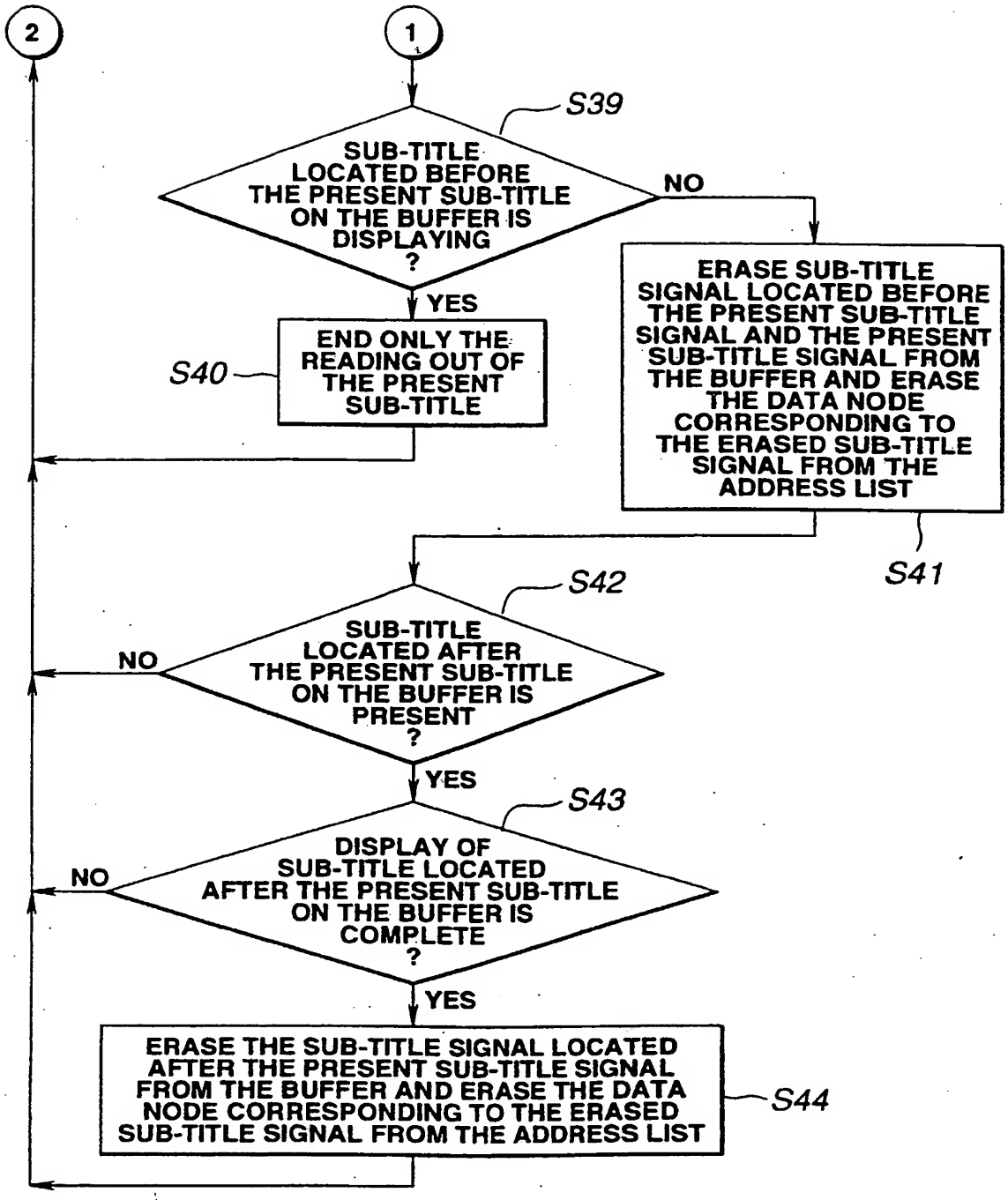

FIG.15B

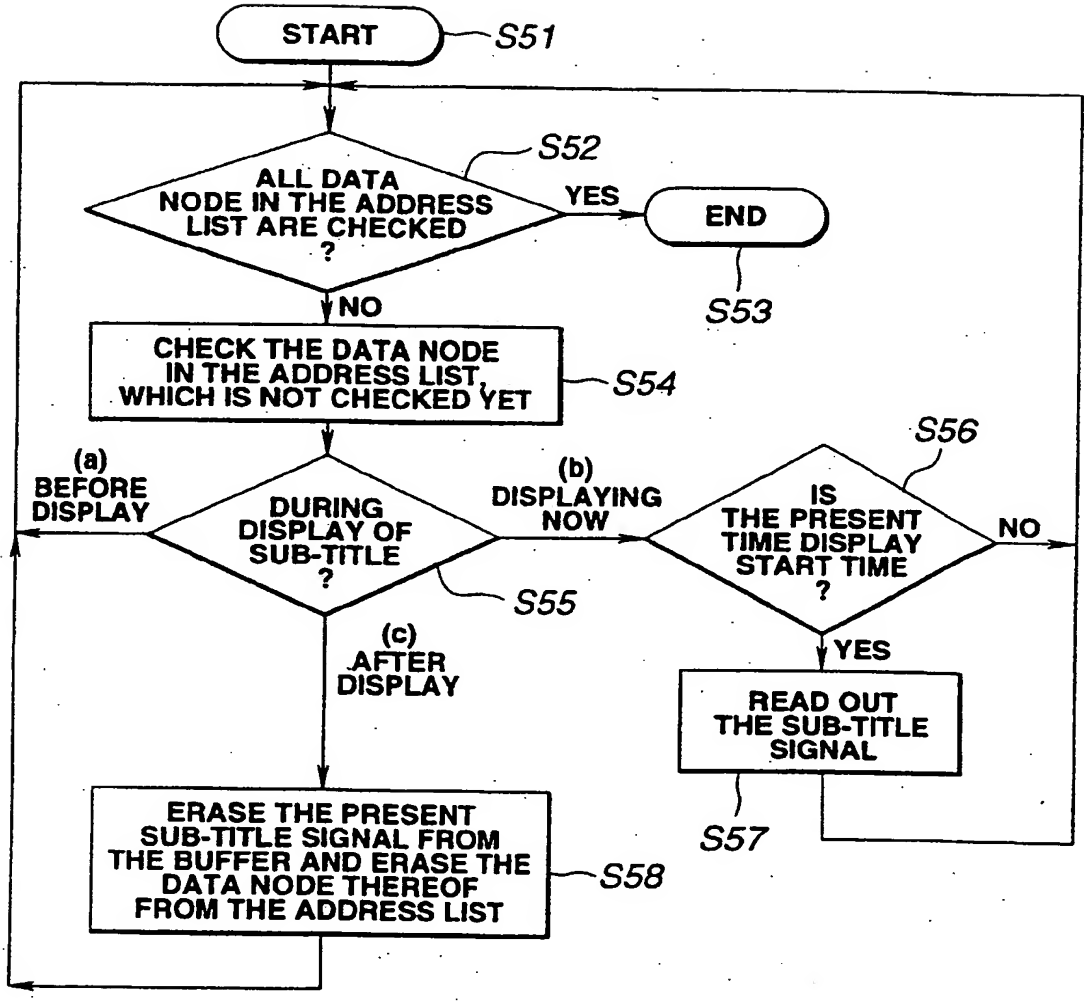

FIG.16

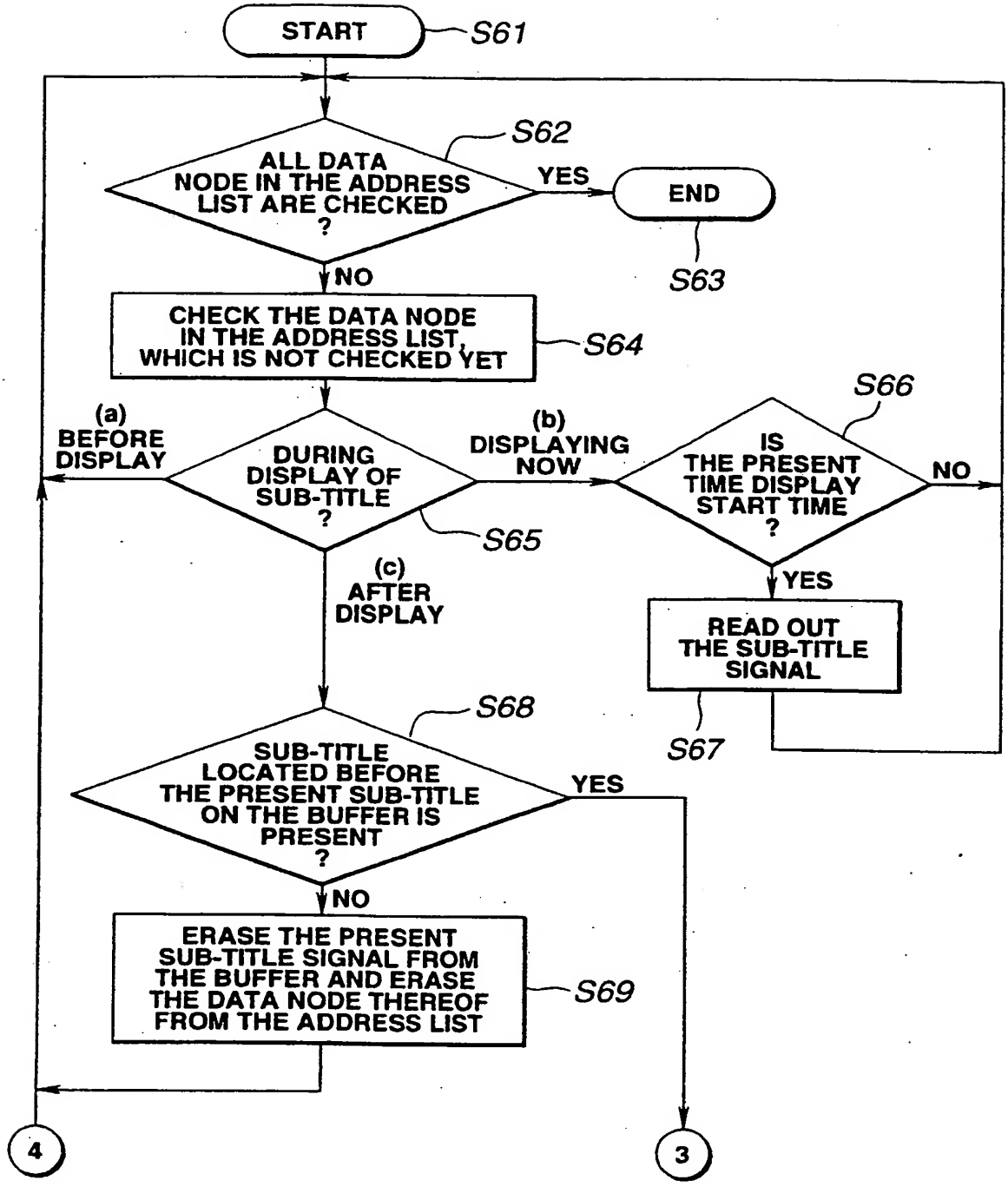

FIG.17A

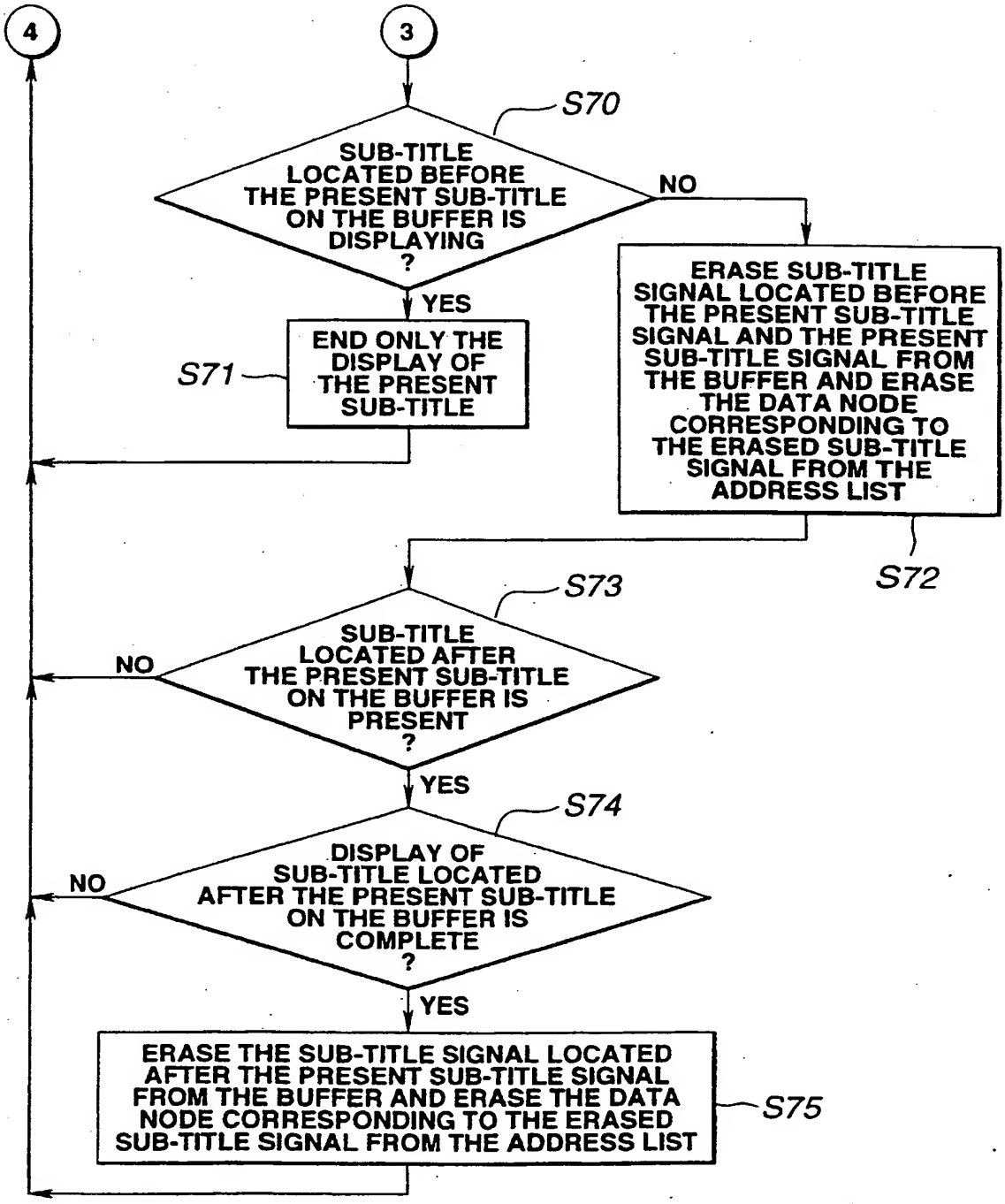

FIG.17B